FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

ATTY. DOCKET NO.	APPLICATION NO.
174/079Re	
APPLICANT: Nghia Tran, et al.	
FILING DATE: October 19, 2001	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DC	Re. 34,808	12/20/94	Hsieh	326	71	
DC	4,032,800	06/28/77	Dröscher et al.	307	296	
DC	4,472,647	09/18/84	Allgood et al.	307	475	
DC	4,527,079	07/02/85	Thompson	307	475	
DC	4,625,129	11/25/86	Ueno	307	446	
DC	4,783,607	11/08/88	Hsieh	307	475	
DC	4,791,312	12/13/88	Weick	307	264	
DC	4,797,583	01/10/89	Ueno et al.	307	475	
DC	4,820,937	04/11/89	Hsieh	307	475	
DC	4,879,481	11/07/89	Pathak et al.	307	465	
DC	4,933,577	06/12/90	Aso	307	465	
DC	4,970,410	11/13/90	Matsushita et al.	307	303	
DC	4,975,602	12/04/90	Nhu	307	475	
DC	4,987,319	01/22/91	Kawana	307	465	
DC	4,994,691	02/19/91	Naghshineh	307	475	
DC	4,999,529	03/12/91	Morgan, Jr. et al.	307	475	
DC	5,023,488	06/11/91	Gunning	307	475	
DC	5,028,821	07/02/91	Kaplinsky	307	465	
DC	5,034,634	07/23/91	Yamamoto	307	465	
DC	5,132,573	07/21/92	Tsuru et al.	307	475	
DC	5,151,619	09/29/92	Austin et al.	307	475	
DC	5,235,219	08/10/93	Cooperman et al.	307	443	
DC	5,282,271	01/25/94	Hsieh et al.	395	275	
DC	5,300,835	04/05/94	Assar et al.	307	475	
DC	5,311,080	05/10/94	Britton et al.	307	465	
DC	5,317,210	05/31/94	Patel	307	465	

EXAMINER Daniel O. Chang DATE CONSIDERED 10/29/02

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DC	5,332,935	07/26/94	Shyu	307	475	
DC	5,374,858	12/20/94	Elmer	327	333	
DC	5,428,305	06/27/95	Wong et al.	326	75	
DC	5,428,800	07/27/95	Hsieh et al.	395	775	
DC	5,534,794	07/09/96	Moreland	326	63	
DC	5,534,798	07/09/1996	Phillips et al.	326	108	
DC	5,589,783	12/31/96	McClure	326	71	
DC	5,612,637	03/18/97	Shay et al.	326	86	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
DC	01-274512	11/02/89	Japan				
DC	02-013124	01/17/90	Japan				
DC	02-161820	06/21/90	Japan				
DC	04-223617	08/13/92	Japan				
DC	0 358 501	09/07/89	EPO				
DC	0 426 283 B1	05/08/91	EPO				
DC	0 544 461 A2	06/02/93	EPO				
DC	0 608 515 A1	08/03/94	EPO				
DC	0 616 431 B1	09/21/94	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
DC	B.A. Chappell, et al., "Fast CMOS ECL Receivers with 100mV Worst-Case Sensitivity" IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, February 1988, pp. 59-66.
DC	F. Claude, "Cross-boundry PLDs", Semiconductor Currents, June 1991, pp. 9-10.

EXAMINER David O. Clay DATE CONSIDERED 10/29/02

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EXAMINER INITIAL	
DC	Carlo Guardiani, et al., "Applying a submicron mismatch model to practical IC design" IEEE 1994 Custom Integrated Circuits Conference, 1994, pp. 297-300.
DC	Bill Gunning, et al., "A CMOS Low-Voltage-Swing Transmission-Line Transceiver" IEEE International Solid-State Circuits Conference, 1992, pp. 58-59.
DC	Andrew Haines, "Field-programmable gate array with non-volatile configuration", Microprocessors and Microsystems, Vol. 13, No. 5, June 1989, pp. 305-312.
DC	H.I. Hanafi, et al., "Design and Characterization of CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance" , IEEE Journal of Solid-State Circuits, Vol. 27, No. 5, May 1992, pp. 783-785.
DC	"IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications", June 1992, pp. 1-5.
DC	K. Knack, "Debunking High-Speed PCB Design Myths", ASIC & EDA, July 1993, pp. 12-26.
DC	M.J.M. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer", IEEE Journal of Solid-State Circuits, Vol. 30, No.7, July 1995, pp. 823-825.
DC	M.J.M. Pelgrom, et al., "Matching Properties of MOS Transistor", IEEE Journal of Solid-State Circuits, Vol. 24, No.5, October 1989, pp. 1433-1440.
DC	B. Prince, et al., "ICS going on a 3-V diet", IEEE Spectrum, May 1992, pp. 23-25.
DC	A.L. Roberts, "Session XIX: High Density SRAMs", IEEE International Solid-State Circuits Conference, February 1987, pp. 252-254.
DC	R. Senthinathan, "Application Specific CMOs Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise", IEEE Journal of Solid-State Circuits Conference, Vol. 28, No. 12, December 1993, pp. 1383-1388.
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DC	M. Ueda, "A 3.3V ASIC for Mixed Voltage Applications with Shut Down Mode", IEEE Custom Integrated Circuits Conference, 1993, pp. 25.5.1 - 25.5.4.
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DC	T.T. Vu., "A Gallium Arsenide SDFL Gate Array with On-chip RAM", IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 1, February 1984, pp. 10-22.
DC	J. Williams, "Mixing 3-V and 5-V Ics", IEEE Spectrum, March 1993, pp.40-42.

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